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(54) **CONTROL CIRCUIT THAT OPERATES ON PULSE-WIDTH MODULATED SIGNALS.**

(57) A control circuit having a drive circuit that operates in response to pulse-width modulated control signals to control a unit to be controlled. A first d-c voltage level is applied by a bias circuit (15) to an analog control signal. A triangular wave voltage or a saw-tooth wave voltage which is obtained by a comparison voltage generator circuit (17) and of which the amplitude change depending upon the change in the power-source voltage, is superposed on a second d-c voltage level that is higher than the first d-c voltage level, and on a third d-c voltage level that is lower than the first d-c voltage level, the second and the third d-c voltage levels being obtained by dividing the power-source voltage. The analog control signal to which the first d-c voltage level is added, and the triangular wave or saw-tooth wave voltage which is superposed on the second and third d-c voltage levels are compared by level comparator circuits (30, 31) that produce first and second pulse-width controlled signals which drive a drive circuit (32) to control a unit to be controlled (43). Therefore, the control operation is stably carried out without requiring any particular constant-voltage source. Further, the power consumption by the unit to be controlled is efficiently reduced.

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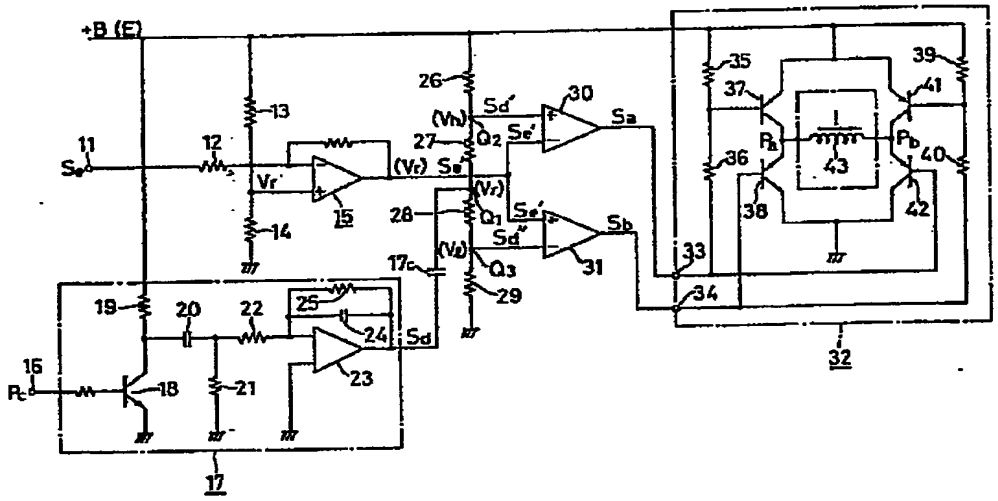
Croydon Printing Company Ltd.

FIG. 3


+B (E)
11
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15
Vr
26
27
28
Q1
Q2
Q3
29
30
31
Sa
Sb
Sd'
Sd''
Se'
(Vh)
(Vl)
(Vr)
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S P E C I F I C A T I O N

CONTROL CIRCUITS OPERATING WITH PULSE-WIDTH MODULATED SIGNALS

Technical Field

The present invention relates to a control circuit operating with a pulse-width modulated signal, in which the current or voltage supply to a unit to be driven from a driving circuit portion provided for driving the unit to be driven is controlled in accordance with a control signal formed into a pulse-width modulated signal.

Technical Background

There has been proposed a signal reproducing system for reproducing information signals such as video signals and audio signals from a disc-shaped recording medium having record tracks in which the information signals are recorded with an alignment of pits. In the signal reproducing system, the record tracks on the recording medium are scanned by a light beam and variations which the light beam is subjected to are detected to reproduce the recorded information signals. Such a recorded information signal reproducing system is known as a video disc system, a digital audio disc system or the like. A reproducing apparatus for such a system is required to have automatic control operations respectively for maintaining the light beam, which is directed to

the recording medium to scan the record tracks thereon, in correct tracking relation to each record track and for focusing the light beam properly on the record tracks while scanning the record tracks with the light beam. These automatic control operations for causing the light beam to impinge correctly upon the record tracks and for focusing the light beam properly on the record tracks are called tracking control and focusing control, respectively, and are usually carried out by driving an optical device, such as a lens or a mirror, partially constituting an optical head for causing the light beam to be directed to the record medium to control the position thereof with control signals which are obtained respectively in response to the tracking condition and the focusing condition of the light beam on the record medium.

In order to drive the optical device for such tracking control or focusing control, the reproducing apparatus is provided with a driving circuit which is operative to supply a driving current or voltage to an actuating device provided for the optical device in accordance with the control signal. As for driving the optical device in this way, it has been proposed to employ a control circuit operating with a pulse-width modulated signal which is operative to supply the control signal formed into a pulse-width modulated signal to the driving circuit with the intention of improving efficiancy in driving.

A proposed control circuit which operates with a pulse-width modulated signal and employed for such a use as mentioned above is shown in Fig. 1 of the accompanying drawings. In the circuit of Fig. 1, an analog control signal Se as shown in Fig. 2A obtained for the tracking control is supplied to a terminal 1, and a triangular waveform signal Ss having a constant amplitude and a constant cyclic period, as shown also in Fig. 2A, is supplied to a terminal 2. These analog control signal Se and triangular waveform signal Ss are compared in voltage level with each other at a level comparator 3, and a pulse-width modulated signal S_1 which is given a high level h when the voltage level of the analog control signal Se is higher than that of the triangular waveform signal Ss and a low level ℓ when the voltage level of the analog control signal Se is equal to or lower than that of the triangular waveform signal Ss so as to be formed into a series of pulses each having the width varying in response to variations in the voltage level of the analog control signal Se, as shown in Fig. 2B, is derived from the level comparator 3. The pulse-width modulated signal S_1 is supplied directly to one of the input terminals of a driving circuit 5 and also to an inverter 4. The pulse-width modulated signal S_1 supplied to the inverter 4 is subjected to level inversion thereat so as to be formed into an inverted pulse-width modulated signal S_2 as shown in Fig. 2C and

this inverted pulse-width modulated signal S_2 is supplied to the other of the input terminals of the driving circuit 5.

The driving circuit 5 is operative to supply a driving current to an electromagnetic coil 6 constituting an actuating device for driving the optical device, for example, the lens or the mirror as aforementioned, and comprises a pair of complementary transistors 7 and 8 having respective bases connected in common to the input terminal to which the pulse-width modulated signal S_1 is supplied and another pair of complementary transistors 9 and 10 having respective bases connected in common to the input terminal to which the inverted pulse-width modulated signal S_2 is supplied. The transistors 7 and 8 are connected between a power source $+B_0$ and the ground with respective emitters coupled in common to make a connection point P_1 and the transistors 9 and 10 are also connected between the power source $+B_0$ and the ground with respective emitters coupled in common to make a connection point P_2. The electromagnetic coil 6 is connected between the connection points P_1 and P_2.

With the configuration described above, when the pulse-width modulated signal S_1 has the high level h and the inverted pulse-width modulated signal S_2 has the low level ℓ, the transistors 7 and 10 are made conductive so that the electromagnetic coil 6 is supplied with a first driving current flowing therethrough from

the connection point P_1 to the connection point P_2, and when the pulse-width modulated signal S_1 has the low level $\underline{\ell}$ and the inverted pulse-width modulated signal S_2 has the high level $\underline{h}$, the transistors 8 and 9 are made conductive so that the electromagnetic coil 6 is supplied with a second driving current flowing therethrough from the connection point P_2 to the connection point P_1. Accordingly, each duration in which the first driving current flows through the electromagnetic coil 6 and each duration in which the second driving current flows through the electromagnetic coil 6 are varied in response to the variations in the voltage level of the analog control signal Se.

However, in such a proposed control circuit, control gain G is determined to be in proportion to the ratio of a voltage E_0 of the power source $+B_0$ to the amplitude (peak to peak value) of the triangular waveform signal Ss, and therefore the control gain G is undesirably varied to exert a baneful influence upon the current supply to the electromagnetic coil 6 by the circuit if the voltage E_0 of the power source $+B_0$ varies. Accordingly, it is necessary to provide a stabilized power source supplying a constant voltage as the power source $+B_0$. In such a case, since the power source $+B_0$ constitutes a power supply for the driving circuit 5 which requires large power, the stabilized power source which is able to supply large power is required and

this results is a problem that a burden on the circuit construction is increased. Further, in the proposed control circuit described above, the electromagnetic coil 6 is supplied always with the first or second driving current through the driving circuit 5 when the control circuit operates, and consequently the electromagnetic coil 6 causes considerably large power consumption.

Disclosure of the Invention

Accordingly, it is an object of the present invention to provide a control circuit operating with a pulse-width modulated signal which controls stably a driving circuit portion for driving a unit to be driven to operate in response to a pulse-width modulated control signal without requiring a power source stabilized particularly for supplying a constant voltage and is able to reduce effectively power consumption at the unit to be driven.

According to an aspect of the present invention, there is provided a control circuit operating with a pulse-width modulated signal, which comprising; a reference voltage producing circuit portion for generating a triangular or saw-toothed waveform voltage signal having an amplitude varying in response to variations in a power supply voltage, a first level comparing circuit portion for comparing the voltage level of an analog control signal provided with a first DC voltage

level with the voltage level of the triangular or saw-toothed waveform voltage signal superposed on a second DC voltage level obtained by dividing the power supply voltage to be higher than the first DC voltage level and for producing a first pulse-width modulated control signal resulting from the level comparison carried out therein, a second level comparing circuit portion for comparing the voltage level of the triangular or saw-toothed waveform voltage signal superposed on a third DC voltage level obtained by dividing the power supply voltage to be lower than the first DC voltage level with the voltage level of the analog control signal provided with the first DC voltage and for producing a second pulse-width modulated control signal resulting from the level comparison carried out therein, and a driving circuit portion operative to drive a unit to be driven and supplied with the first and second pulse-width modulated control signals.

In the control circuit thus constituted in accordance with the present invention, the driving circuit portion is controlled to drive the unit to be driven in accordance with each pulse-width modulated control signal, which is obtained by converting the analog control signal into a pulse-width modulated control signal by the aid of the triangular or saw-toothed waveform voltage signal, with the control gain maintained to be substantially constant even if the power supply voltage is varied. Accordingly,

it is not necessary to provide for the driving circuit portion any stabilized power source capable of supplying large power with the intention of maintaining the control gain to be constant and the driving circuit portion is appropriately controlled without requiring a power source stabilized particularly, so that the burden on the circuit configuration is considerably lightened. Further, the unit to be driven is supplied intermittently with a driving current through the driving circuit portion when the control circuit operates, and therefore the power consumption caused by the unit to be driven is effectively reduced.

Breif Description of the Drawings

Fig. 1 is a schematic circuit diagram showing a previously proposed control circuit which operates with a pulse-width modulated signal;

Figs. 2A to 2C are waveform diagrams used for explaining the operation of the control circuit shown in Fig. 1;

Fig. 3 is a schematic circuit diagram showing an embodiment of control circuit operating with a pulse-width modulated signal according to the present invention; and

Figs. 4A to 4D are waveform diagrams used for explaining the operation of the embodiment shown in Fig. 3.

Embodiment most preferable for working of the Invention

Now, a preferred embodiment of the present invention will be described in detail with reference to the accompanying drawings hereinafter.

Fig. 3 shows an example of the control circuit operating with a pulse-width modulated signal according to the present invention. In this example, for example, the analog control signal Se as aforementioned is supplied to a terminal 11. The analog control signal Se from the terminal 11 is supplied through a resistor 12 to a biasing circuit 15 to which a biasing voltage level Vr obtained by dividing a power supply voltage E of the power source +B is applied, and at the output terminal of the biasing circuit 15, a modified analog control signal Se' which corresponds to the analog control signal Se superposed on the biasing voltage level Vr is obtained.

On the other hand, a clock pulse signal Pc having a constant cyclic period and a constant pulse-width of each pulse therein is supplied through a terminal 16 to a charging and discharging circuit 17 employing a Miller integrator. The charging and discharging circuit 17 has a switching transistor 18 which has a base supplied with the clock pulse signal Pc and is turned on and off selectively in response to the clock pulse signal Pc. An emitter of the switching transistor 18 is grounded and a collector of the switching transistor 18 is connected to the power source +B through a resistor 19. A sereis

connection of a capacitor 20 and a resistor 21 is connected between the collector of the switching transistor 18 and the ground, and the connection point between the capacitor 20 and the resistor 21 is connected through a resistor 22 to one of input terminals of an operational amplifier 23. The other of the input terminals of the operational amplifier 23 is grounded and a parallel connection of a capacitor 24 and a resistor 25 is connected between an output terminal and the above mentioned one input terminal of the operational amplifier 23, so that the Miller integrator is formed.

In the charging and discharging circuit 17 thus constituted, the switching transistor 18 is made conductive for a constant duration cyclically at fixed periods by the clock pulse signal Pc, and a rectangular pulse voltage corresponding to the power supply voltage E is obtained cyclically at fixed periods at the collector of the swiching transistor 18 whenever the switching transistor 18 is made nonconductive. In accordance with this rectangular pulse voltage obtained at the collector of the swiching transistor 18, charging and discharging are substantially carried out alternately in the Miller integrator including the operational amplifier 23 provided with the parallel connection of the capacitor 24 and the reseistor 25, and as a result of this, a triangular waveform voltage signal Sd having a cyclic period corresponding to the cyclic period of the clock pulse signal Pc and an amplitude (peak

to peak value) proportional to the power supply voltage E is generated at the output terminal of the operational amplifier 23, namely, the output terminal of the charging and discharging circuit 17. That is, the charging and discharging circuit 17 produces the triangular waveform voltage signal Sd which has the amplitude varying in response to variations in the power supply voltage E when the power supply voltage E is varied.

A voltage divider comprising a series connection of resistors 26, 27, 28 and 29 is connected between the power source +B and the ground. This voltage divider is so arranged as to produce a DC voltage level Vr which coincides with the biasing voltage level Vr applied to the biasing circuit 15 as mentioned above at a connection point Q_1 between the resistors 27 and 28, a DC voltage level Vh which is higher by a predetermined value corresponding to a half of the amplitude of the triangular waveform voltage signal Sd than the DC voltage level Vr at a connection point Q_2 between the resistors 26 and 27, and a DC voltage level $V\ell$ which is lower by the predetermined value corresponding to a half of the amplitude of the triangular waveform voltage signal Sd than the DC voltage level Vr at a connection point Q_3 between the resistors 28 and 29. With such an arrangement, the difference between the DC voltage levels Vh and $V\ell$ (Vh - $V\ell$) is set to be coincident with the amplitude of the triangular waveform voltage signal Sd.

The output terminal of the charging and discharging circuit 17 is connected through a capacitor 17c to the connection point Q_1 of the voltage divider, so that the triangular waveform voltage signal Sd is supplied to the connection point Q_1. Accordingly, a modified triangular waveform voltage signal Sd which corresponds to the triangular waveform voltage signal Sd superposed on the DC coltage level Vh, as shown in Fig. 4A, is obtained at the connection point Q_2, and another modified triangular waveform voltage signal Sd' which corresponds to the triangular waveform voltage signal Sd superposed on the DC voltage level $V\ell$, as shown also in Fig. 4A, is obtained at the connection point Q_3. In such a situation, the bottom level of the modified triangular waveform voltage signal Sd' and the top level of the modified triangular waveform voltage signal Sd" are coincident with the DC voltage level Vr. Although the DC voltage levels Vr, Vh and $V\ell$ vary respectively so that the difference between the DC voltage levels Vh and Vr (Vh - Vr) and the difference between the DC voltage levels Vr and $V\ell$ (Vr - $V\ell$) are varied when the power supply voltage E varies, the amplitude of the triangular waveform voltage signal Sd also varies in response to the variations in the power supply voltage E and consequently such relationship among the modified triangular waveform voltage signals Sd' and Sd" and the DC voltage level Vr as shown in Fig. 4A and described above is maintained

notwithstanding the variations in the power supply voltage E.

The modified triangular waveform voltage signal Sd' obtained at the connection point Q_2 and the modified analog control signal Se' obtained at the output terminal of the biasing circuit 15 are supplied to a level comparator 30 to be compared in voltage level with each other therein, and a pulse-width modulated signal Sa which is given the high level h when the voltage level of the modified triangular waveform voltage signal Sd' is higher than that of the modified analog control signal Se' and the low level ℓ when the voltage level of the modified triangular waveform voltage signal Sd' is equal to or lower than that of the modified analog control signal Se' so as to be formed into a signal containing pulses each having the width varying in response to variations in the voltage level of the modified analog control signal Se', as shown in Fig. 4B, is derived from the level comparator 30. Further, the modified analog control signal Se' and the modified triangular waveform voltage signal Sd" obtained at the connection point Q_3 are supplied to a level comparing circuit 31 to be compared in voltage level with each other therein, and a pulse-width modulated signal Sb which is given the high level h when the voltage level of the modified analog control signal Se' is higher than that of the modified triangular waveform voltage signal Sd" and the low level ℓ when the voltage level of the modified

analog control signal Se' is equal to or lower than that of the modified triangular waveform voltage signal Sd" so as to be formed into a signal containing pulses each having the width varying in response to variations in the voltage level of the modified analog control signal Se', as shown in Fig. 4C, is derived from the level comparator circuit 31.

The pulse-width modulated signals Sa and Sb thus obtained are supplied to input terminals 33 and 34 of a driving circuit 32, respectively. The driving circuit 32 comprises a pair of transistors 37 and 38 having respective collector-emitter paths coupled in series through a connection point Pa and connected between the power source +B and the ground and another pair of transistors 41 and 42 having respective collector-emitter paths coupled in series through a connection point Pb and connected between the power source +B and the ground in parallel with the collector-emitter paths of the transistors 37 and 38 coupled in sereis. Between the connection points Pa and Pb, an electromagnetic coil 43 for driving a unit to be driven, for example, an optical device such as the lens or mirror as aforementioned is connected. Further, bases of the transistors 37 and 41 are connected to the power source +B through resistors 35 and 39, respectively.

With such an arrangement, the pulse-width modulated signal Sa from the input terminal 33 is supplied

to the base of the transistor 37 through a resistor 36 and to the base of the transistor 42 directly. Similarly, the pulse-width modulated signal Sb from the input terminal 34 is supplied to the base of the transistor 41 through a resistor 41 and to the base of the transistor 38 directly.

In the driving circuit 32 thus constituted, the transistors 37 and 42 are made nonconductive when the pulse-width modulated signal Sa has the high level h and made conductive when the pulse-width modulated signal Sa has the low level ℓ, and similarly the transistors 41 and 38 are made nonconductive when the pulse-width modulated signal Sb has the high level h and made conductive when the pulse-width modulated signal Sb has the low level ℓ. As understood clearly from Figs. 4B and 4C, when the pulse-width modulated signal Sa has the low level ℓ, the pulse-width modulated signal Sb has the high level h, and when the pulse-width modulated signal Sb has the low level ℓ, the pulse-width modulated signal Sa has the high level h. Accordingly, when the pulse-width modulated signal Sa has the low level ℓ, only the transistors 37 and 42 are made conductive so that the electromagnetic coil 43 is supplied with a driving current I flowing therethrough in the direction from the connection point Pa to the connection point Pb, as indicated with an arrow in Fig. 3, and when the pulse-width modulated signal Sb has the low level ℓ, only the transitors 41 and 38 are made conductive so that the electromagnetic coil 43 is supplied

with the driving current I flowing therethrough in the direction from the connection point Pb to the connection point Pa opposite to the direction indicated with the arrow in Fig. 3. To the contrary, when both the pulse-width modulated signals Sa and Sb have the high level h, each of the transistors 37, 38, 41 and 42 is made nonconductive and therefore the electromagnetic coil 43 is not supplied with any driving current. In such a manner, the current supply to the electromagnetic coil 43 by the driving circuit 32 is controlled in accordance with the pulse-width modulated signals Sa and Sb, so that the driving current I flows intermittently through the electromagnetic coil 43, as shown in Fig. 4D, and each duration in which the driving current I flows continuously through the electromagnetic coil 43 and the direction of the driving current I flowing through the electromagnetic coil 43 are varied in response to the voltage level of the analog control signal Se.

As described above, since the electromagnetic coil 43 is supplied intermittently with the driving current I, the power consumption at the electromagnetic coil 43 is effectively reduced, and since the amplitude of each of the modified triangular waveform voltage signals Sd' and Sd" is varied in response to the variations in the power supply voltage E, the ratio of the power supply voltage E to the amplitude of each of the modified triangular waveform voltage signals Sd' and

Sd" is kept almost constant, so that the control gain for the driving circuit 32 is maintained to be substantially constant notwithstanding the variations in the power supply voltage E.

Incidentally, although the triangular waveform voltage signal Sd is obtained from the charging and discharging circuit 17 to serve as a reference coltage signal used for converting the analog control signal Se into the pulse-width modulated signals Sa and Sb in the embodiment described above, it is possible to have such a modification that a saw-toothed waveform voltage signal is employed, instead of the triangular waveform voltage signal Sd, to serve as the reference voltage signal used for converting the analog control signal Se into the pulse-width modulated signals Sa and Sb.

Applicability for Industrial Use

The control circuit according to the present invention is capable of controlling various movable devices requiring relatively large power for driving to be driven with improved driving efficiency, and is therefore suitable not only for being used to drive the optical device such as the lens or mirror employed in the reproducing apparatus for the video disc system, the digital audio disc system or the like, as aforementioned, but also for being used to drive any other actuator, for example, a solenoid plunger employed in various electronic

apparatus.

Claims for Patent

1. A control circuit operating with a pulse-width modulated signal comprising;

biasing circuit means (15) for providing with a first DC voltage levle to an analog control signal,

voltage generating circuit means (26, 27, 28, 29) for producing a second DC voltage level higher than the first DC voltage level and a third DC voltage level lower than the first DC voltage level by dividing a power supply voltage,

reference voltage producing circuit means (17) for generating a triangular or saw-toothed waveform voltage signal having an amplitude varying in response to variations in the power supply voltage,

first level comparing circuit means (30) for comparing the voltage level of the analog control signal provided with the first DC voltage level with the voltage level of the triangular or saw-toothed waveform voltage signal superposed on the second DC voltage level and for producing a first pulse-width modulated control signal resulting from the level comparison carried out therein,

second level comparing circuit means (31) for comparing the voltage level of the triangular or saw-toothed waveform voltage signal superposed on the third DC voltage level with the voltage level of the analog control signal provided with the first DC voltage and for producing

a second pulse-width modulated control signal resulting from the level comparison carried out therein, and

driving circuit means (32) for driving a unit to be driven in accordance with the first and second pulse-width modulated control signals.

2. A control circuit according to claim 1, wherein said biasing circuit means (15) is operative to produce the first DC voltage level with level variations caused in response to the variations in the power supply voltage and supply the analog control signal superposed on the first DC voltage level from the output terminal thereof.

3. A control circuit according to claim 2, wherein said voltage generating circuit means (26, 27, 28, 29) comprises a first resistor (26), a second resistor (27), a third resistor (28) and a fourth resistor (29) connected in sereis with a first connection point which is provided between said first and second resistors (26, 27) and at which the second DC voltage level is obtained, a second connection point which is provided between said third and fourth resistors (28, 29) and at which the third DC voltage level is obtained, and a third connecting point which is provided between said second and third resistors (27, 28) and to which the output terminal of said reference voltage producing circuit means (17) is connected.

4. A control circuit according to claim 1 or 2, wherein said reference voltage producing circuit means (17) comprises a charging and discharging circuit employing a Miller integrator and including a switching transistor (18) which is turned on and off alternately with a predetermined clock pulse signal supplied thereto.

5. A control circuit according to claim 3, wherein a pair of input terminals of said first level comparing circuit means (30) are coupled with the connecting point provided between said first and second resistors (26, 27) and the output terminal of said biasing circuit means (15), respectively, and a pair of input terminals of said second level comparing circuit means (31) are coupled with the output terminal of said biasing circuit means (15) and the second connecting point provided between said third and fourth resistors (28, 29), respectively.

6. A control circuit according to claim 1, 2 or 5, wherein said driving circuit means (32) comprises a plurality of swiching elements (37, 38, 41, 42) each of which is supplied with the first or second pulth-width modulated signal to be turned on and off alternately for supplying intermittently with a driving current to said unit to be driven.

FIG. 1

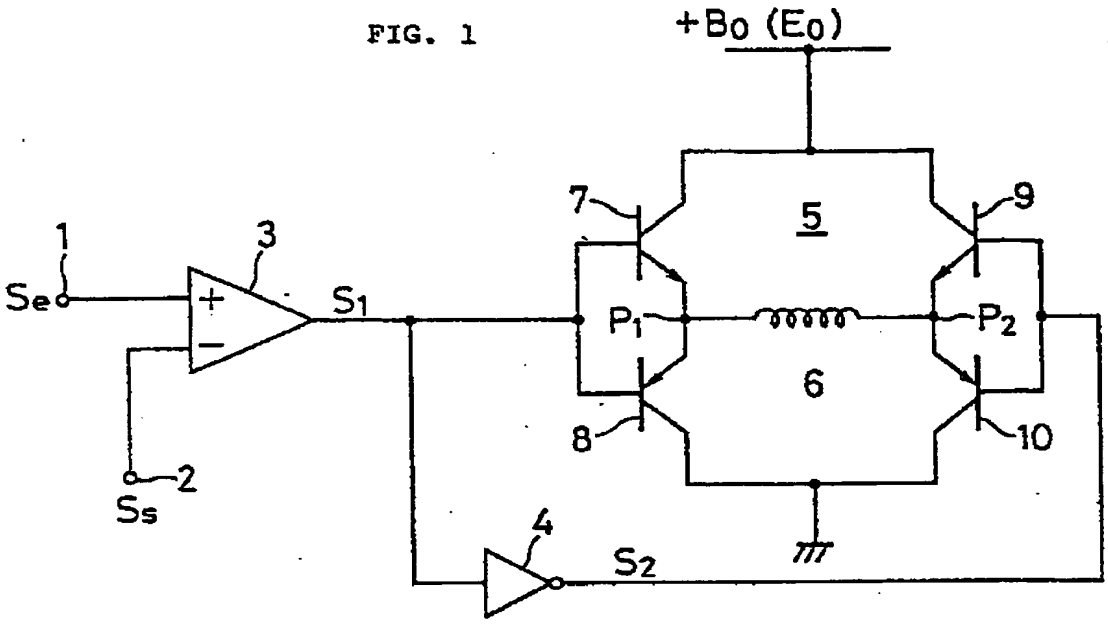


FIG. 2A

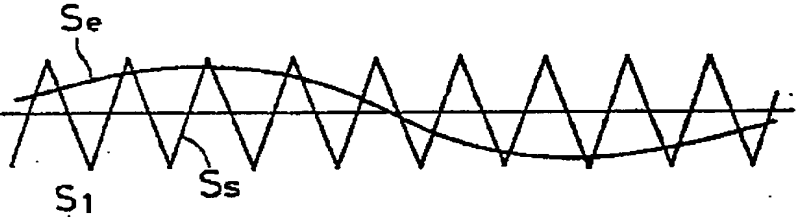


FIG. 2B

FIG. 2C

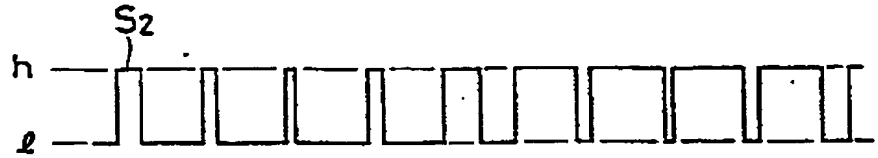
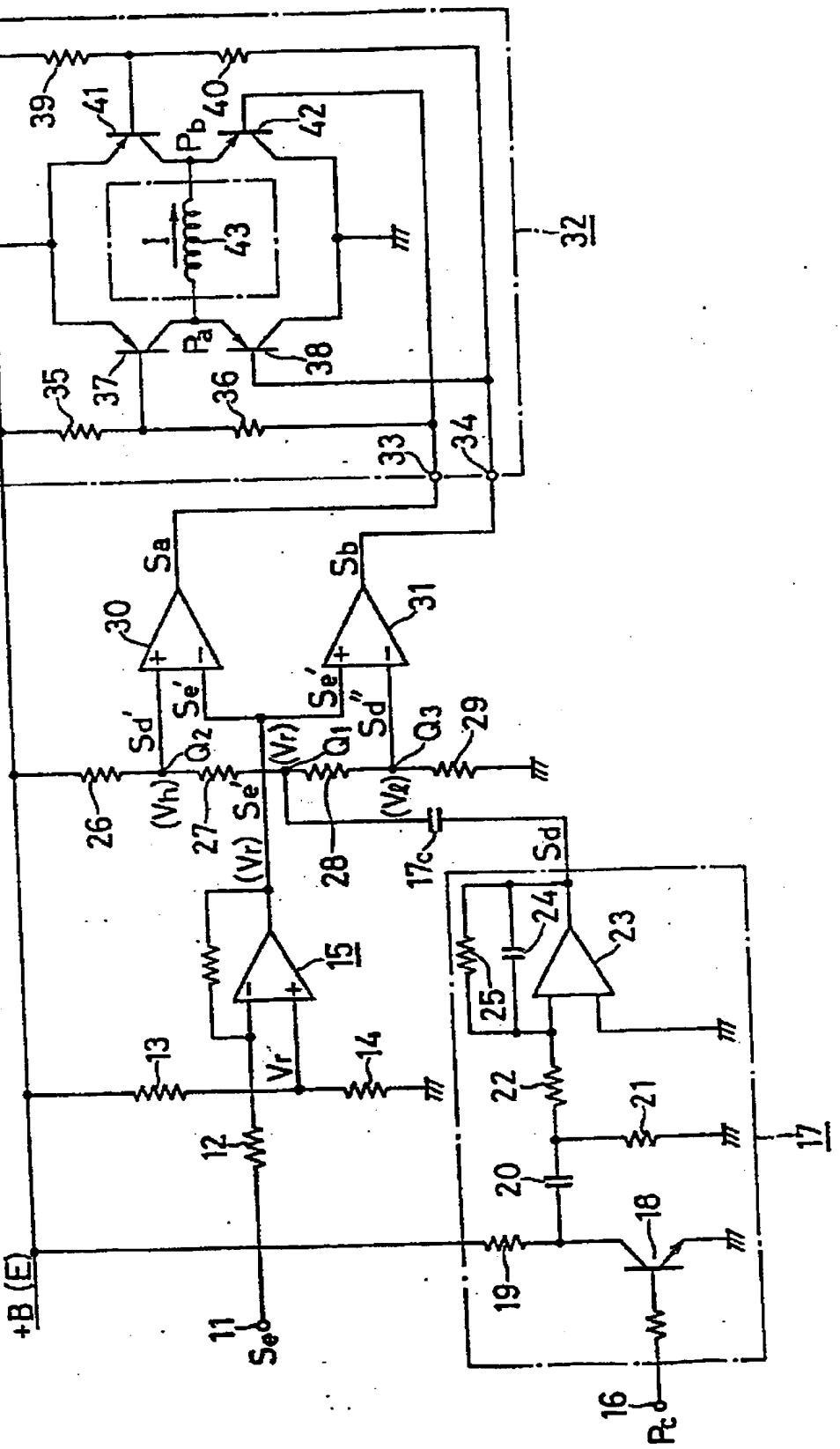


FIG. 3


32
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43
38
37
36
35
33
34
Sa
Sb
30
31
Sd'
Se'
Q2
Q1
Sd''
Q3
29
26
27
28
17c
Sd
24
23
25
15
13
14
12
22
21
17
20
18
19
+B (E)
11
Se
16
Pc

FIG. 4A

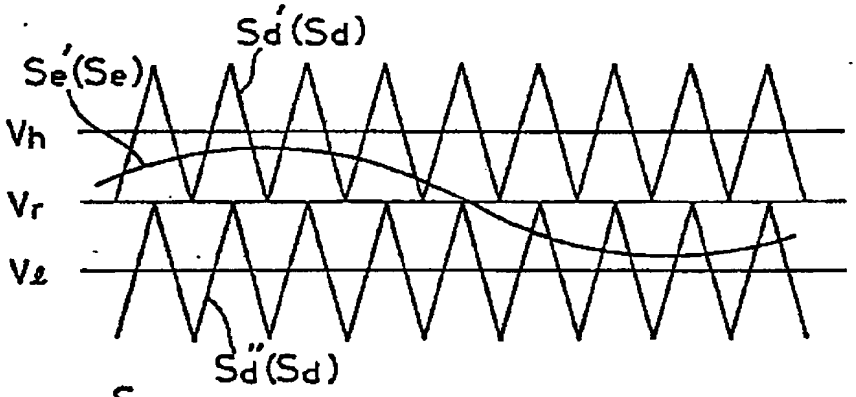

FIG. 4B

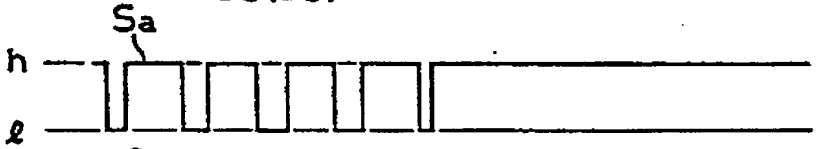

FIG. 4C

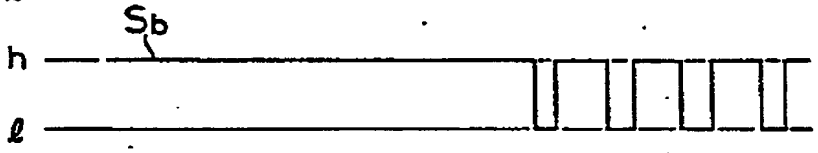

FIG. 4D

INTERNATIONAL SEARCH REPORT

International Application No. PCT/JP85/00119

0183849

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl[4] H03F3/217, H03K7/08

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC	H03F3/217, H03K7/08

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

Jitsuyo Shinan Koho 1926 - 1985
Kokai Jitsuyo Shinan Koho 1971 - 1985

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category*	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	JP, B2, 56-27001 (Victor Co. of Japan, Ltd.), 22 June 1981 (22. 06. 81), Figs. 3 to 6 & JP, A, 51-12758	1 - 5
Y	JP, B2, 56-27001 (Victor Co. of Japan, Ltd.), 22 June 1981 (22. 06. 81), Figs. 3 to 6	6
Y	JP, Y1, 43-2802 (Trio-Kenwood Corp.), 6 February 1968 (06. 02. 68) (Family : none)	6

* Special categories of cited documents: [15]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
May 28, 1985 (28. 05. 85)	June 10, 1985 (10. 06. 85)
International Searching Authority [1]	Signature of Authorized Officer [20]
Japanese Patent Office	